Dynamic adjusting threshold voltage scheme for low power FinFet circuits

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Abstract

Dynamic-adjusting threshold-voltage scheme (DATS) for the design of an independent-gate (IG)-mode fin-type field-effect transistor (FinFET) circuit is discussed in this work. . DATS makes use of the intrinsic advantage of the IG-mode FinFET to adjust the threshold of the front gate with the back-gate bias adaptively according to the operating frequency. Consequently, the power consumption, especially leakage power of the circuit, would be reduced effectively without circuit performance deterioration. By further comparing the circuits where the DATS scheme is employed with the circuits that do not adopt the scheme, the power optimization levels with different path delays in different operating frequency ranges are discussed in detail. A design instance of DATS based on digitally controlled phase-locked loop is implemented with an ASAP 7-nm FinFET model. Simulation results illustrate that by employing DATS the power reduction could be up to 30% in the best case. Keywords: Dynamic-adjusting threshold-voltage scheme(DATS); fin-type field-effect transistor(FinFET).

1 Introduction

A phase-locked loop (PLL) is widely employed in wireline and wireless communication systems. The poor device matching and leakage current vary the common-mode voltage of a ring-based voltage-controlled oscillator (VCO) wide frequency range. It may limit the oscillation frequency range of a VCO and causes a VCO not to oscillate in a worst case. To realize a wide-range PLL, the divider following a VCO should operate between the highest and lowest frequencies. When a PLL works at a higher frequency which the static circuits cannot operate, dynamic circuits are needed.

A true-single-phase-clocking (TSPC) divider is widely used to realize a prescaler for this PLL. A TSPC prescaler must work over a wide frequency range to cover the process and temperature variations. For a TSPC prescaler, the undesired leakage currents may limit its frequency range or alter the original states of the floating nodes to have a malfunction. The leakage current and current mismatch in a charge pump (CP) will degrade the reference spur and jitter significantly.In the previous method to overcome the above problems, a self-healing divide-by-4/5 prescaler and a self-healing VCO used. A time-to digital converter (TDC) and a 4-bit encoder are used to quantize the phase error and digitally calibrate the CP.In the existing method the key parameter is to be changed is the modulus value of the prescaler. By changing the value of the prescaler the PLL frequency range will be extended.

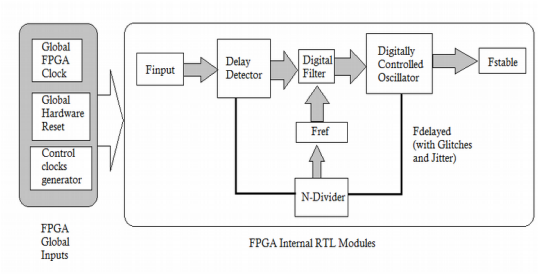
2. PLL Building Blocks

A conceptual block diagram of a typical PLL is shown in Figure. It consists of five blocks: VCO, feedback frequency divider, phase frequency detector (PFD) / charge pump (CP), low-pass loop filter (LPF) and crystal oscillator (Xtor).

3. PROPOSED SYSTEM

The proposed system consists of Dynamic adjusting threshold voltage is generated through various sources. The variable voltage is helpful to generate multiple operations at the same time.FinFet is the concept which consume less power, the modified SOC platform enable the FPGA system to work in reliable manner even at fast varying frequencies.The proposed system consists of Time varying PLL design with reconfigurable threshold levels.

Proposed Block diagram



4. High frequency divider

A high frequency divider in a wide band PLL system needs high frequency capability as well as wide frequency range. Injection locked frequency dividers have been proposed due to their high frequency capability [Rategh99]. However, the drawback of narrow input frequency range or locking range makes it unsuitable in this wide band system design. Therefore, a DFF-based frequency divider has been chosen to be the high frequency divider design. The D Flip-Flop consists of two D-Latch, which are driven by the same clock signal but with opposite phases. The inverted output of the DFF is fed back to the input to generate waveform with half of the input frequency.

Though we have chosen the DFF-based structure, the logic style to implement the D-Latch and other accessory circuits is still to be decided. The major concern is high speed. Without using the normal complementary CMOS logic style, very fast logic style, SCL, has been used to successfully implement a fast frequency divider up to very high frequency [Wohlmuth02]. Besides high frequency capability, we also benefit from its low noise level coupled to the substrate, which will be shown later. Furthermore, the differential nature of SCL also reduces the complexity of the logic implementation. For example, one can have signals with both phases simultaneously without the use of an inverter.

5.Elementary SCL cell design

A buffer is the elementary SCL cell. The approach used in its design is basis for the designs of more complex logics.

The main concerns of this circuit include propagation delay, power consumption, and output voltage swing, while taking bias current variation into consideration. As can be seen from the schematic, an SCL buffer consists of three parts: bias current source, the NMOS driving pair and the last is the PMOS load. We will look at the detail design considerations and tell how each part contributes relative to our major concerns mentioned above.

The propagation is the most important specification of the design. It consists of two aspects: the falling delay and the rising delay. The falling delay is determined by the discharging current, which is the bias current. And the rising time is determined by

the charging current from the supply through the PMOS load transistor, which can be controlled through the external gate bias voltage.

Power consumption is decided by both supply voltage and bias current. The lower the supply voltage, the lower is the power consumption. However, using too low a supply voltage will make it very hard to put more transistors in stack when more complex logics are required. For bias current, we can pick up the smallest bias current that satisfies the timing requirement.

The voltage swing can determine the dynamic power and also the sensitivity to noise. In this topology, the maximum output is always the supply voltage. And the minimum output level is decided by the product of the bias current and the resistance of the load PMOS transistor.

One of the most significant advantages of SCL over complementary CMOS logic is its low transition current spike. To make the bias current source more like an ideal source, or to make the output resistance of the current source larger, two transistors in stack are used. To completely switch the bias current from branch to the other, the output swing cannot be too low. Or equivalently speaking, the driving pair has to be strong enough to have low enough turn off voltage, V_{dsat}.

It has a voltage swing of less than 0.4 V and a bias current of about 101 μA. And the bias current transient variation is less than 2%, which is measured from the peak of the swing from the static value

6. Programmable divider

The foundation of a programmable divider is a dual-modulus prescaler and an accumulator. The prescaler can divide the input signal frequency by N or $N+1$ depending on a control signal. And this control signal is from the accumulator. The accumulator has two data input, A and B, which satisfy the relationship $A \leq B$. The accumulation starts at 0 and with the control signal's initial value of logic "0", which means the divider number is $N+1$. When the accumulator reaches A, the control signal turns into logic "1" meaning a divider number of N. This operation lasts until the accumulator counts to B, then the accumulator goes back to 0 and the control signal becomes logic "0" again. If the output of the accumulator is used as the total divider output, then the total divider number is $N_{tot} = A\ (N+1) + (B-A)\ N = A + BN$.

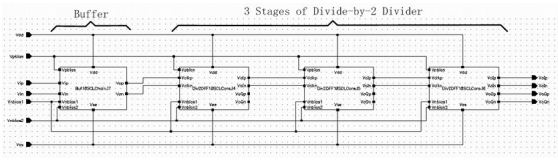
7. SCL high frequency divide-by-8 divider

It consists of three cascaded divide-by-2 divider with each has the same structure and the preceding buffer is used to convert the VCO output voltage level to the SCL voltage level.

The output frequency of the divide-by-8 divider will be 1/8 of the VCO output frequency. And its output is then fed to the input the programmable divider.

8.Phase-select divide-by-1/1.25 prescaler

Phase-select-based dual modulus prescaler has the advantages of higher



maximum input frequency and only the first stage of the circuit working at the maximum frequency comparing to the traditional gating technology [Craninckx96]. The four input signals are at the same maximum frequency but with phase shift. When the "Mode" signal keeps low, the output keeps connecting to only one input, and we get a divide-by-1

9.Noise transfer function and noise shaping

Noise is shaped by the function (1-$J(z)$), which is called the noise shaping function. This filter can reduce the error $E(z)$. Especially at low frequencies a large reduction is obtained. Total amount of the quantization error is found by integrating ()()()$zEzJ\cdot-1$ over the signal bandwidth f_b. $f_b$is also the PLL loop bandwidth. Here we assume that any signal outside f_b can be completely removed by the LPF presented in the loop

10.Band-Searching Scheme

The band-searching scheme used in the Sigma-Delta fractional-N PLL is to help coarse locking of the VCO to the correct band before the beginning of the fine tuning. The VCO has both coarse digital tuning and fine analog tuning. The traditional PLL locking scheme can only change the voltage of the analog tuning node, and do the analog tuning. However, if the digital control bits are not staying at the correct code, no matter how the analog tuning voltage is changed the VCO cannot be locked to the right frequency. So an additional digital control code locking scheme is required before the analog locking.

The band-searching scheme is indeed another feedback control loop. Since only coarse tuning is required, it provides all digital implementation. That means band-searching scheme is not able to find the exactly correct frequency for the VCO but will help it find the correct frequency range after the coarse tuning step is finished, the band-searching scheme locking loop will be broken, and the traditional locking lock begins to work.

10.1 Principle of band-searching scheme

A PLL with band-searching scheme is a double loop system. Its locking process has two steps. The first step is coarse tuning, i.e. band searching to find out the correct VCO band, and the second step is traditional analog fine tuning.The components outside the dotted line region are the same with those of a normal PLL. Of course, the VCO and the fixed divider are also in the normal loop. Those inside the dotted line region form the band-searching loop. VCO and fixed divider are reused. The D latch and the finite state machine (FSM) are both sequential logics with the clock from the reference clock. The counter counts the output of the latch and acts as a phase accumulator. The counter's reset signal is also the reference clock. The comparator is a combinational logic. It simply compares the result of the counter with desired modulus from system input, and the result of the comparison will be sent to the FSM.

The locking procedure starts from a synchronous reset signal. If the system detects a new modulus input, the *"Hold"* signal becomes low and the system state is reset to the band-searching start state. The switches are controlled to break the normal loop and close the band-searching loop. During this procedure, the analog tuning node of the VCO is disconnected from the output of the LPF. Instead, it is connected to some reference voltage V_{min}. V_{min} is set to the minimum tuning voltage available from the output of the LPF. And the digital control bits are set to all zero which means the lowest frequency band, $Band_0$, is chosen. See Figure 4.3 for the details of VCO tuning

11. CONCLUSION:

The Scheme can dynamically adjust the threshold of the FinFET transistors according to the operating frequency by applying the reverse back-gate BIAS. A design instance based on the digitally controlled PLL is implemented and simulated with the ASAP 7-nm FinFET model. Experimental results illustrate that the scheme can effectively reduce the power consumption up to 30% without deteriorating the performance

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